REMARKS/ARGUMENTS

In this amendment, claims 1, 8, and 24 are amended. No claims are canceled or added. Thus, after entry of this amendment, claims 1-27 will remain pending in the application.

Allowable Subject Matter

Applicants note with appreciation the indicated allowability of claims 10-12, 14-17, 19, and 22.

Rejection under 35 U.S.C. § 103(a), Clauberg, Craft, and Agrawal

Claims 1, 3-8, 18, 20 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Clauberg (US PG Publication 2002/0159483 Al) in view of Craft (US Patent 5,652,878) and in further view of Agrawal et al. (US Patent 6,919,736 Bl), hereinafter Agrawal.

Claims 1-7

Claim 1 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1. For example, claim 1 recites:

> *inputting the parallel bits into a content addressable memory and a first register during a single clock cycle; ...*
>
> *providing a bus configured to receive the parallel bits and output of the first register, wherein the data lines forming the bus are grouped into a plurality of overlapping subsets of the bus that each contain at least one common data line;*
>
> *...*
>
> *providing a set of parallel words stored in the content addressable memory, wherein at least one of the set of parallel words includes a fixed frame alignment detection pattern having a data position;*

A. Combination inputs bits into CAM and first register in different clock cycles

Clauberg discloses deserializing an incoming serial data stream into a 16 bit parallel data stream using a deserializer 206. *See Clauberg*, FIG. 2 and paragraph 31. The 16 bit parallel data output stream is converted by a demultiplexing unit 212 into an unaligned 64 bit word, which is then stored in a register 214. *Id.*, paragraph 32. Over three clock cycles, three 64

bit words are stored in a register 216 to form a 192 bit word. *Id.* An align position detection unit 218 locates the specific bit pattern indicating the beginning of a new frame (e.g., A1A2) by "hunting" along the 192 bit word to find the correct 64 bit section. *Id.* Clauberg does not disclose how the align position detection unit operates. *Id.* An extraction unit 222, extracts the correct 64 bit section of the 192 bit word and sends that to an output port 204. *Id.*

At page 4, the Office Action asserts that register 214 is the first register, and the content addressable memory (CAM) is asserted to be either the storage unit 216 (Clauberg, paragraph 32) or some storage unit after output port 204. In either case, the parallel bits are first input into the register 214 and then at least several clock cycles later the data is input into storage unit 222. *Id.*, paragraph 27. Thus, Clauberg does not teach or suggest *"inputting the parallel bits into a content addressable memory and a first register during a single clock cycle,"* as recited by claim 1. Note that none of the teachings of Craft or Agrawal would alter the organization of registers of Clauberg.

B. Combination does not alter alignment mechanism of Clauberg

Craft teaches a method for compressing data by storing received data and then finding repeated patterns and replacing those matched patterns with a token. *See Craft*, col. 1 lines 24-27. Thus, the token is sent instead of the actual data, effectively compressing the data. *Id.*, col. 1 lines 27-30. Craft improves upon the prior art by using a fixed address scheme that implements a CAM to store the newly received data patterns that are used to find repeated patterns to replace with a token. *Id.*, col. 3 lines 42-50.

Thus, a combination of Craft with Clauberg would add the compression scheme of Craft to the aligned output data of Clauberg so that bandwidth may be more efficiently used. The newly stored data would not have any particular alignment associated with it and would not convey alignment information, but would simply be used to identify data that may be sent as a token as opposed to actual data. Even as noted by the Office Action at page 5, the output of Clauberg "is of a particular type and alignment," which suggests that the alignment would need to have already been detected. Accordingly, the combination does not teach or suggest "*wherein at least one of the set of parallel words includes a fixed frame alignment detection pattern having a data position,*" as recited by claim 1.

C. Combination does not have a bus that receives parallel bits and output of first register and that has overlapping subsets with at least one common data line

In Agrawal, the interconnects of LOSMs 281-284 are shared by CMBs 214 and 215. *See Agrawal*, FIG. 2B and col. 12 lines 35-40. In one case, the opposed CMB's 214, 215 are allowed to make overlapping use of the adjacent HIC's for transferring their respective data bits between them, although overlapping use is not further described. *Id.*, col. 12 lines 49-53.

First, Agrawal teaches that the different interconnects may be used to transfer data in different directions, which is why there is shared (overlapping) use. *Id.*, col. 12 lines 23-27. However, Clauberg requires that data is sent only in one direction, i.e. from input to output. Thus, the concepts are not transferable and the inventions would not be combined.

Secondly, each of the LOSMs 281-284 do not have lines that are part of another LOSM, and thus they do not overlap. *Id.*, FIG. 2B and col. 12 lines 12-35. It is the use of the LOSMs that overlaps and not the LOSMs themselves. This is evident in that the subsets service completely separate I/O terminals. *Id.* In contrast, claim 1 recites "*wherein the data lines forming the bus are grouped into a plurality of overlapping subsets*."

Also, as is plainly apparent from FIG. 2B, LOSMs 281-284 do not all share a common data line. *Id.*, FIG. 2B and col. 12 lines 12-35. In contrast, claim 1 recites "*wherein the data lines forming the bus are grouped into a plurality of overlapping subsets of the bus that each contain at least one common data line*."

Additionally, Agrawal would not change the structure of the registers of Clauberg, which does not have "*a bus configured to receive the parallel bits and output of the first register*," as recited in claim 1. In Clauberg, one bus receives the parallel bits and transmits them to the register 214 and a different second bus transfers the output of register 214 to register 216.

For at least the reasons stated above, Applicant submits that claim 1 and its dependent claims 2-7 are allowable over the cited references.

Claims 8-23

As mentioned above, none of the storage units of any combination would have the CAM receiving the first parallel data output and the output of the shift register in parallel, as recited by claim 8.

Also, as mentioned above, the cited references do not teach or suggest "*wherein the subsets include at least one common data line*," as recited in claim 8.

For at least the reasons stated above, Applicant submits that claim 8 and its dependent claims 9-23 are allowable over the cited references.

Claims 24-27

As mentioned above, the cited reference do not teach or suggest "*a plurality of data word subsets that overlap to include at least one common data bit*," as recited in claim 24.

Also, as mentioned above, the cited reference do not teach or suggest "*wherein each of the fixed frame alignment patterns are part of a respective one of a set of parallel words stored in a the content addressable memory,*" as recited in claim 24.

For at least the reasons stated above, Applicant submits that claim 24 and its dependent claims 25-27 are allowable over the cited references.

Other rejections under 35 U.S.C. § 103(a)

Claims 2, 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Clauberg, Craft, and Agrawal as applied to claims 1 and 8 above, and in further view of Morikawa (US Patent 6,7470,886). Claim 2 depends on claim 1 and claims 9 and 13 depend on claim 8, and thus are allowable for at least the same rationale as these claims.

Morikawa is cited as teaching outputting both the parallel bits and the output of the first register into a plurality of tristate driver circuits. (Office Action page 15). Even assuming that Morikawa teaches this limitation and that there is a motivation to combine, this teaching does not make up for the deficiencies in the other references with respect to these claims.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Clauberg, Craft, and Agrawal as applied to claim 8 above, and in further

view of Veenstra et al., hereinafter Veenstra (US Patent 6,160.41 9). Claims 21 depends upon claim 8 and is allowable for at least the same rationale as claim 8.

Veenstra is cited as teaching making use the circuit in a programmable logic IC implementation. (Office Action page 17). Even assuming that Veenstra teaches this limitation and that there is a motivation to combine, this teaching does not make up for the deficiencies in the other references with respect to these claims.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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